

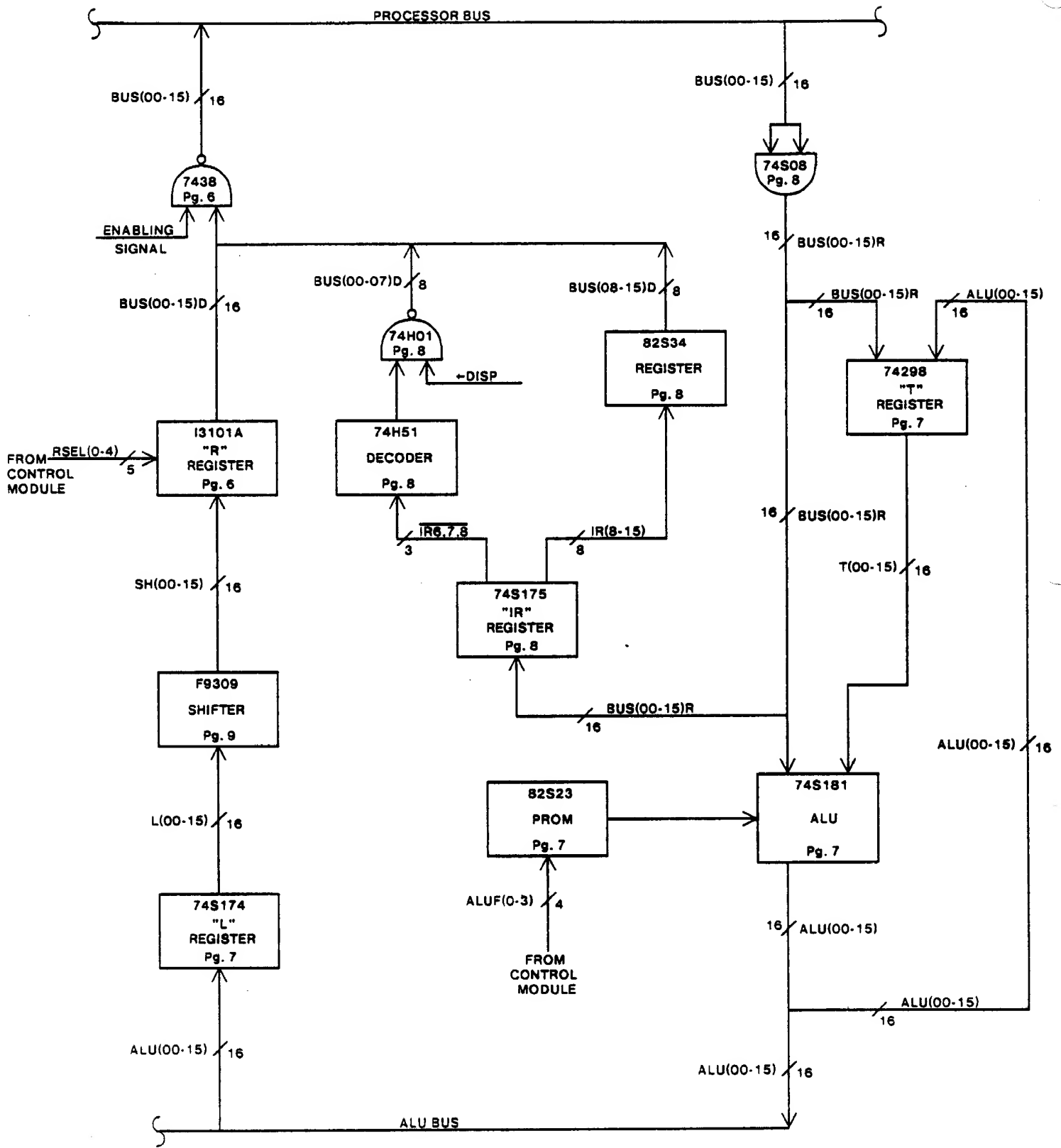
## ARITHMETIC SECTION

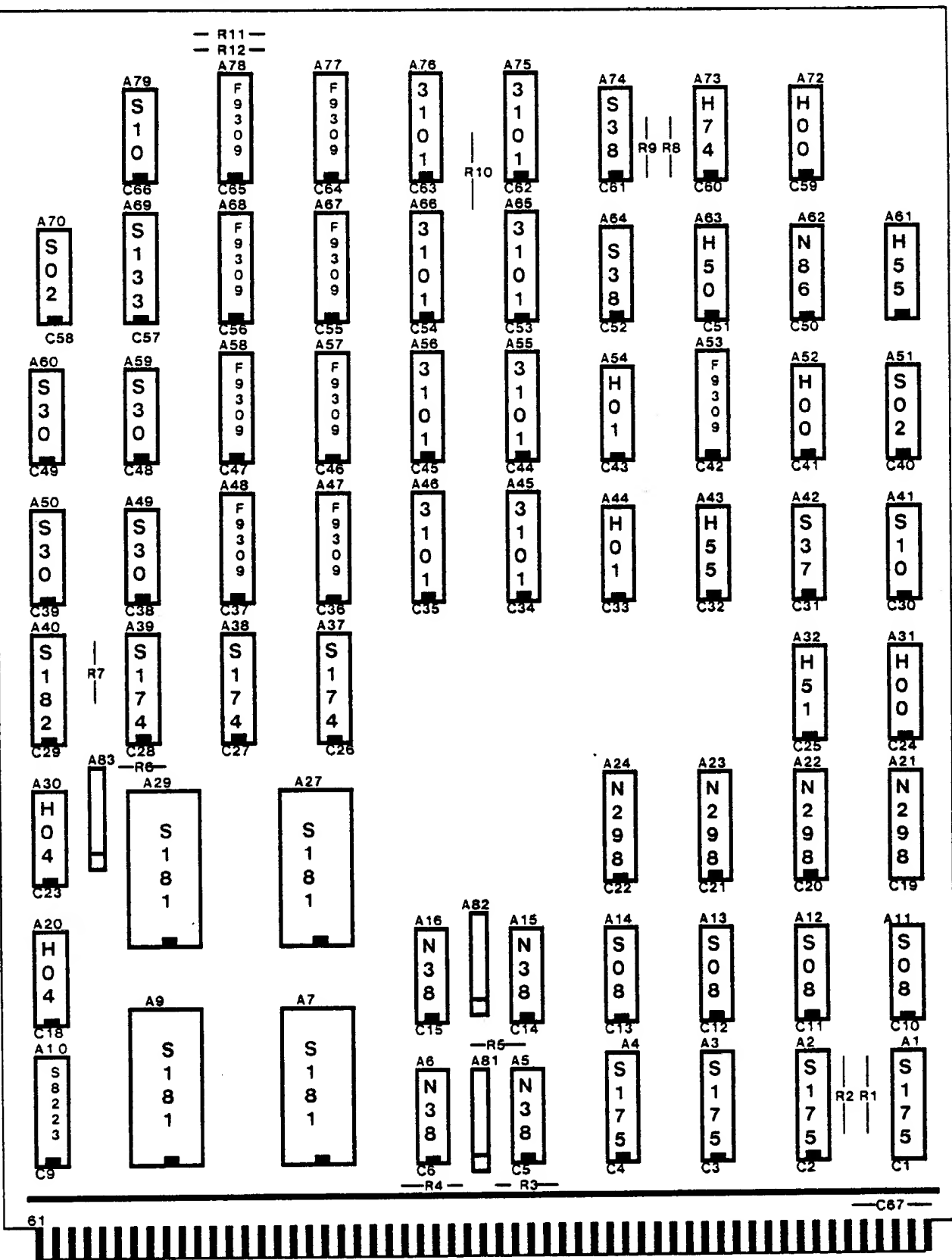
The arithmetic section of the processor consists of two 32-word by 16-bit register files R and S, and five registers, T, L, M, MAR, and IR. The registers are connected to the memory and to an ALU with a 16-bit parallel bus.

The ALU is a SN74181 type, restricted so that it can do only 16 arithmetic and logical functions. The ALU output feeds the L, M, and MAR registers. T may also be loaded from the ALU output under certain conditions. L is connected to a shifter capable of left and right shifts by one place, and cycles of 8. It has a mode in which it does the peculiar 17-bit shifts of the standard instruction set, and a mode which allows double-length shifts to be done.

The IR register is used by the emulator to hold the current emulated instruction.

# ARITHMETIC LOGIC UNIT (ALU)





61

PROPRIETARY NOTE ON SHEET 1 APPLIES TO ALL SHEETS

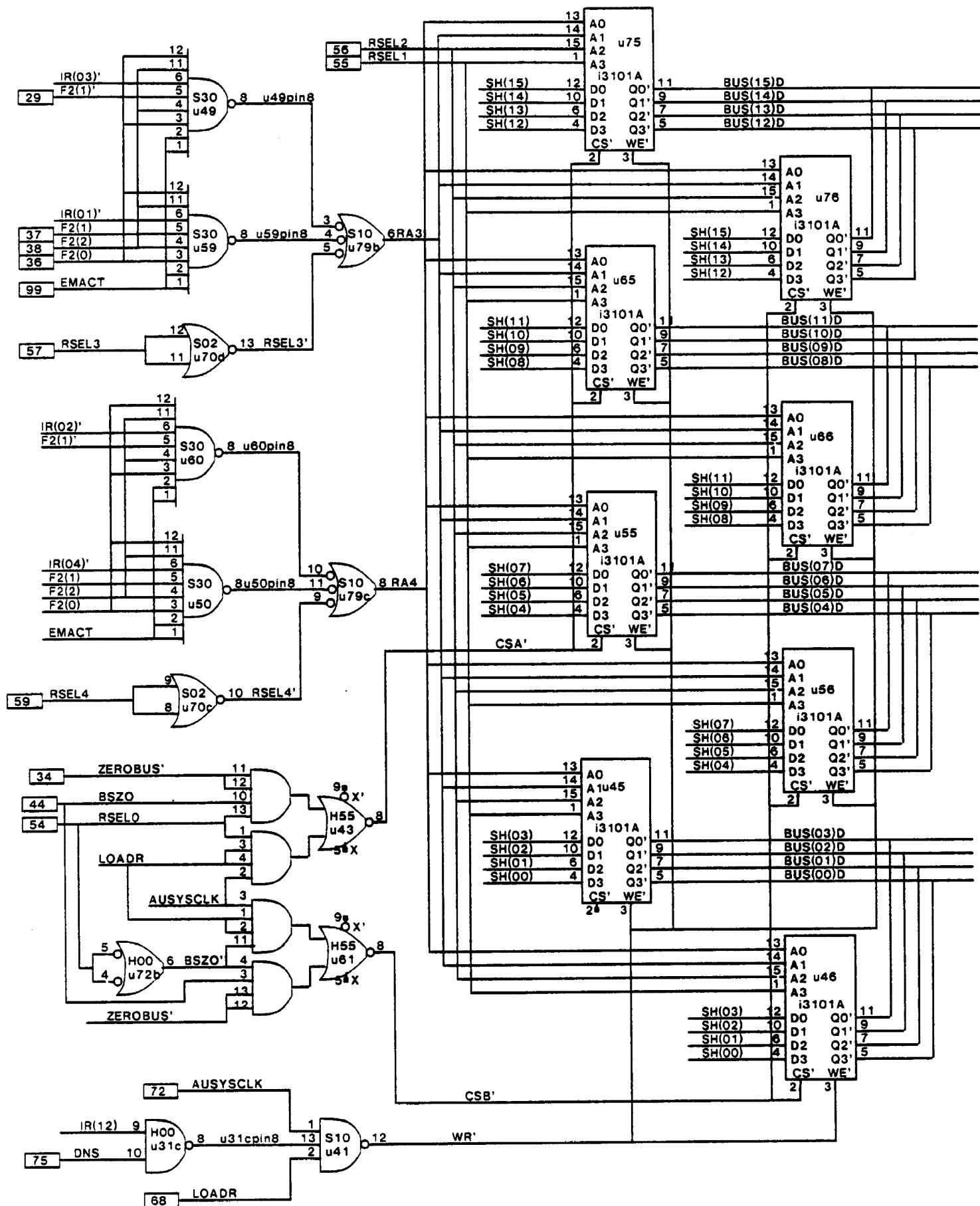
FILE: ALU03.SIL

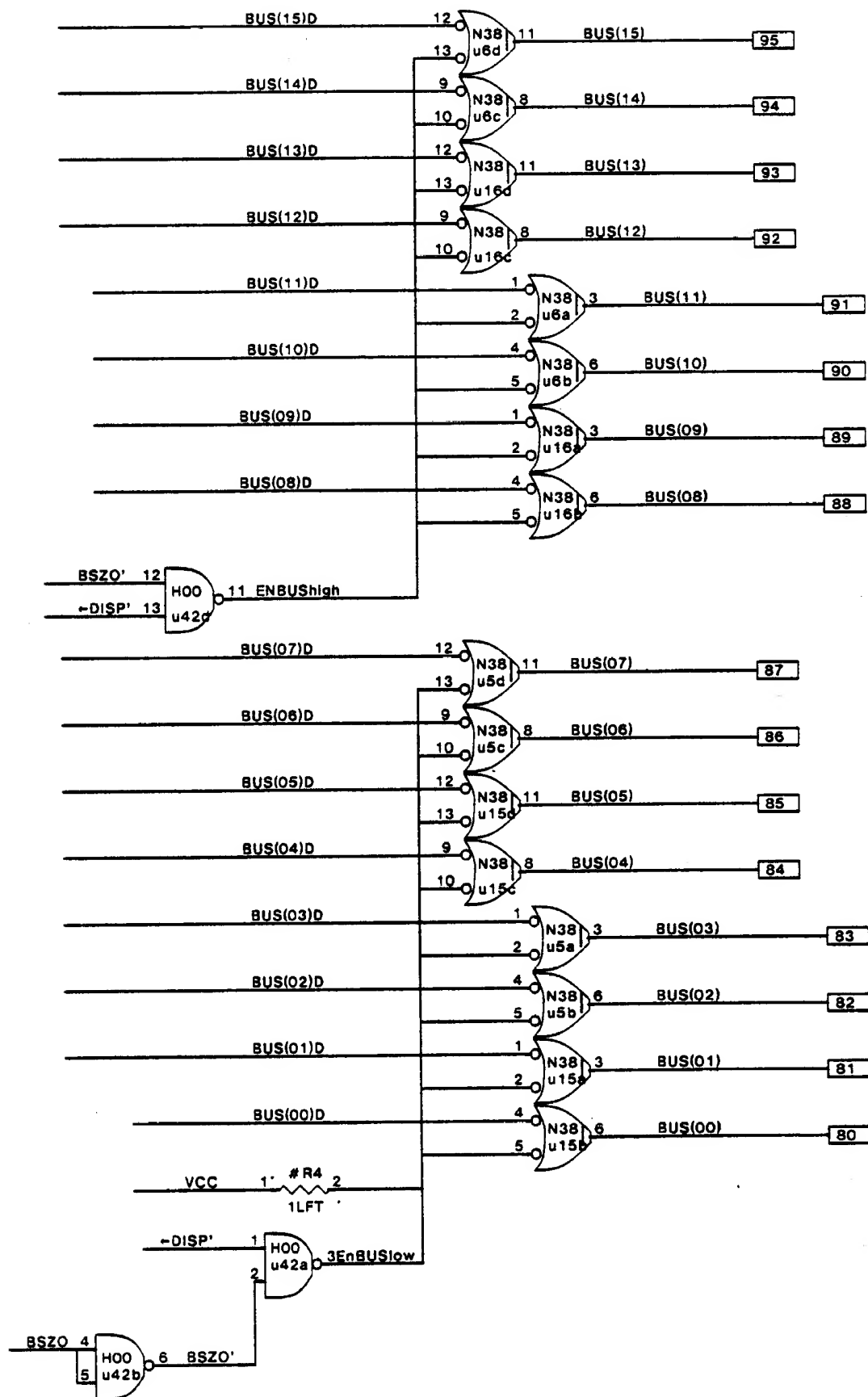
TITLE  
ASSEMBLY, P.W.  
ARITHMETIC LOGIC UNIT (ALU) MODULE

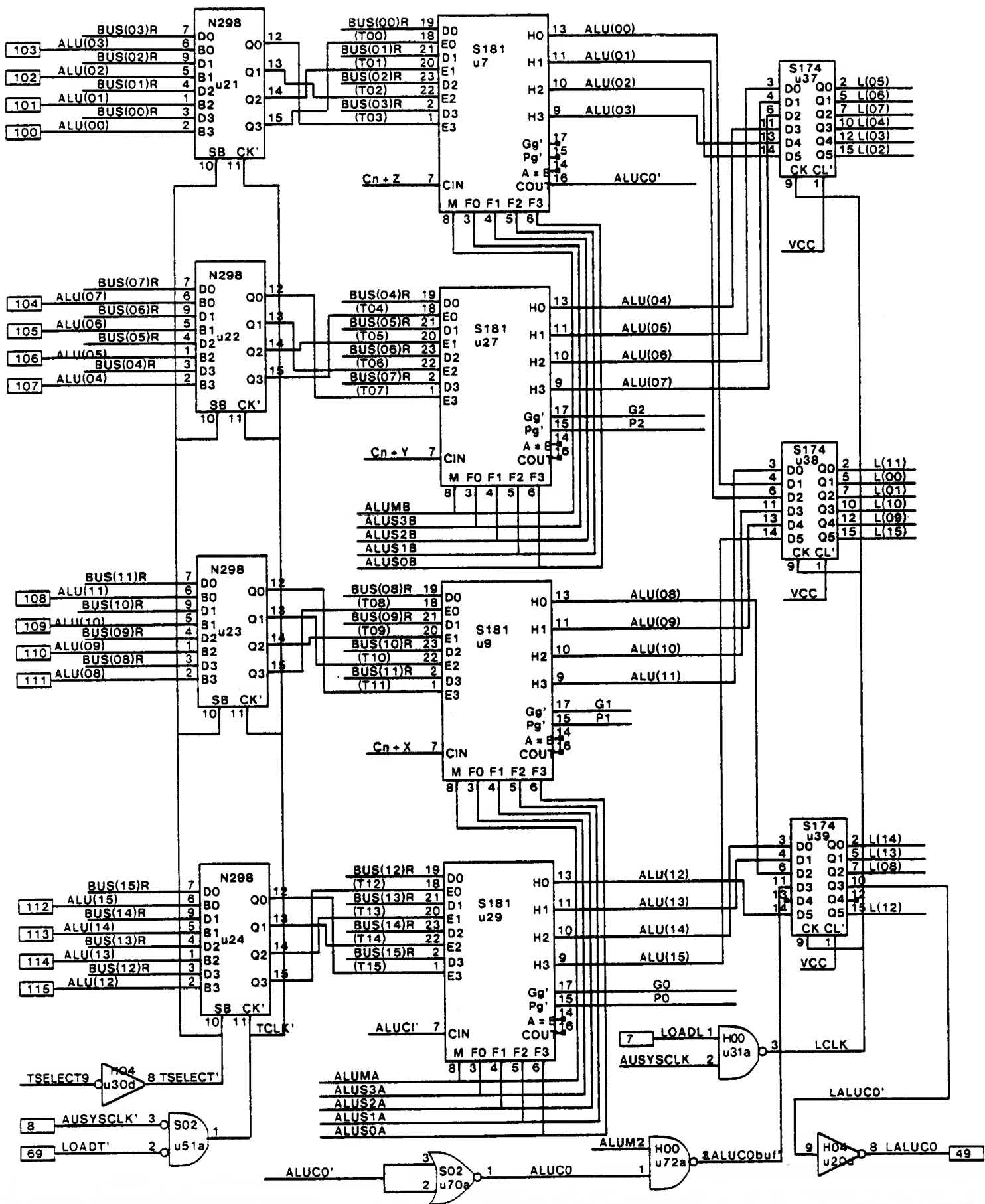
DWG.  
SIZE  
A41

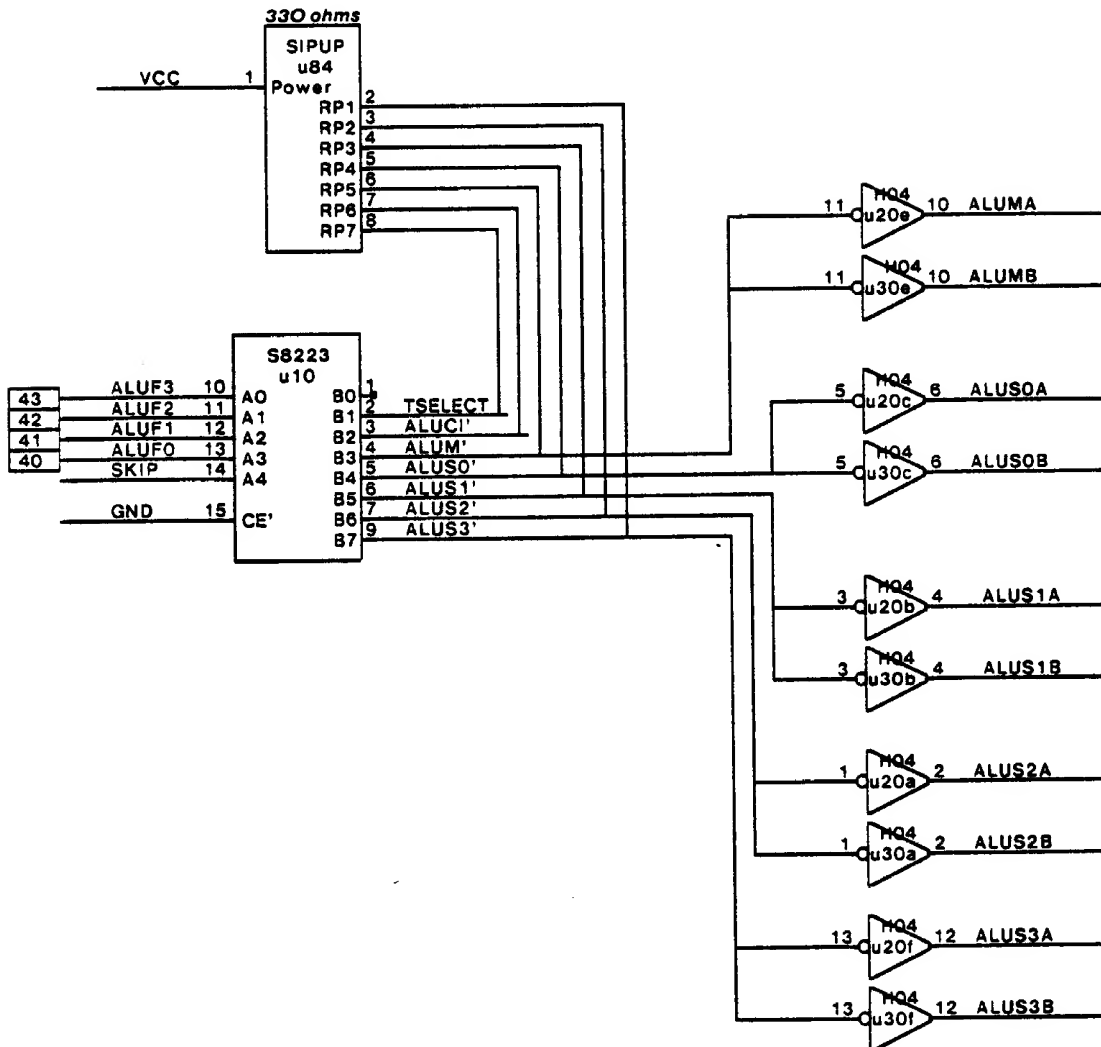
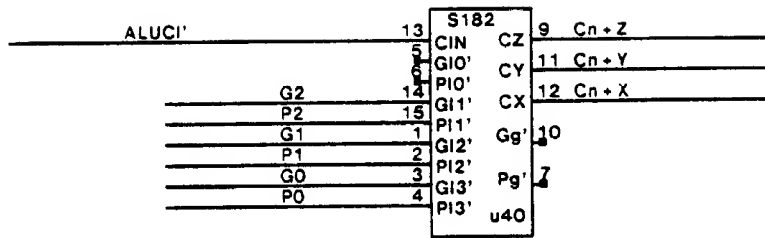
DWG. 218090  
NO.  
SHEET 3 OF 13

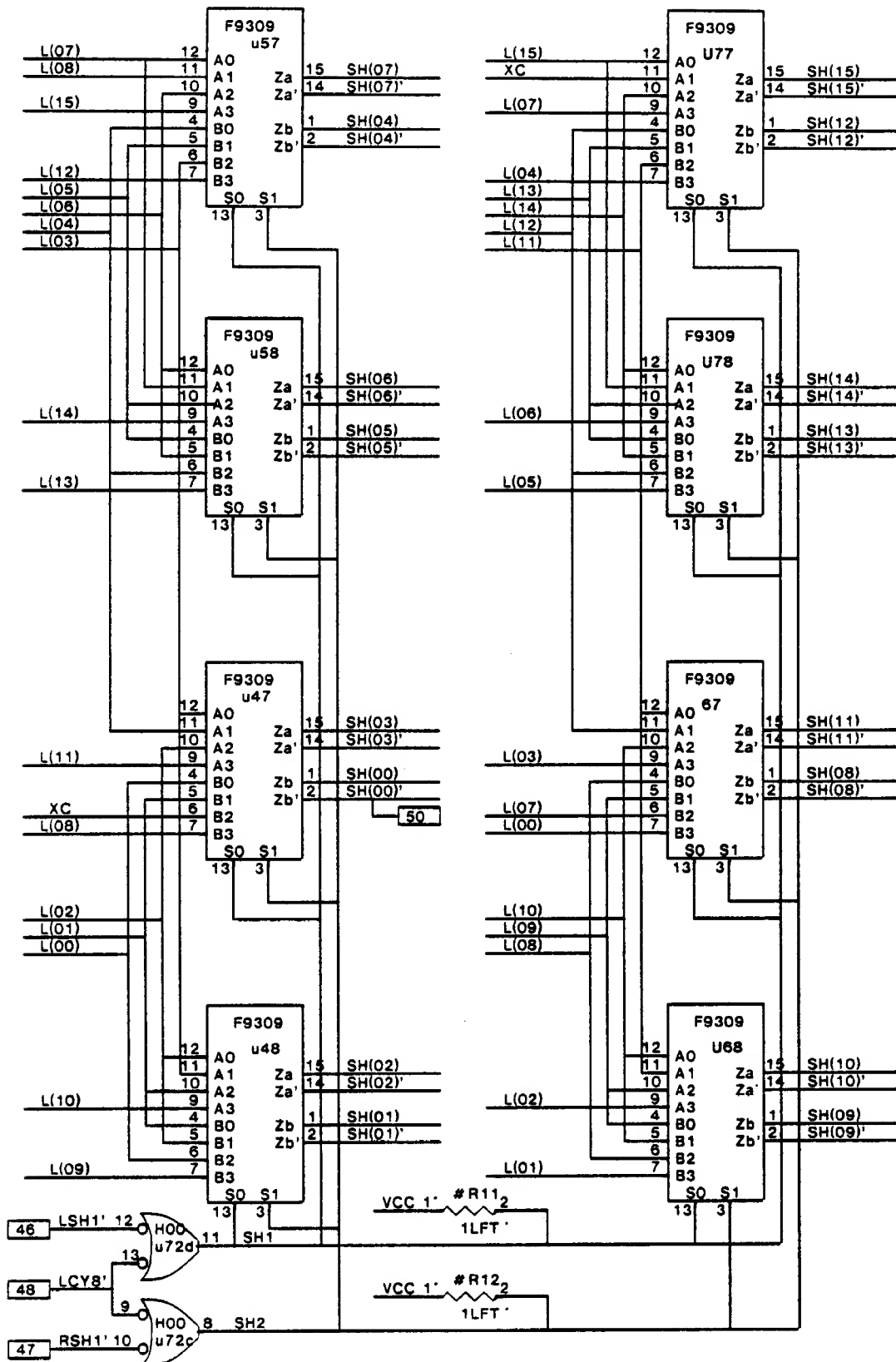
SHEET  
REV.  
A



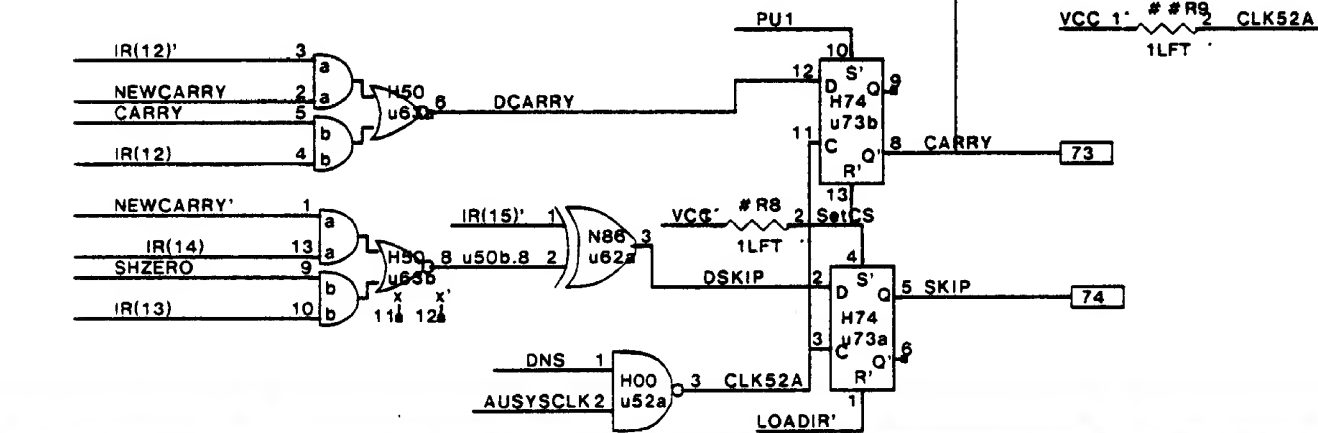
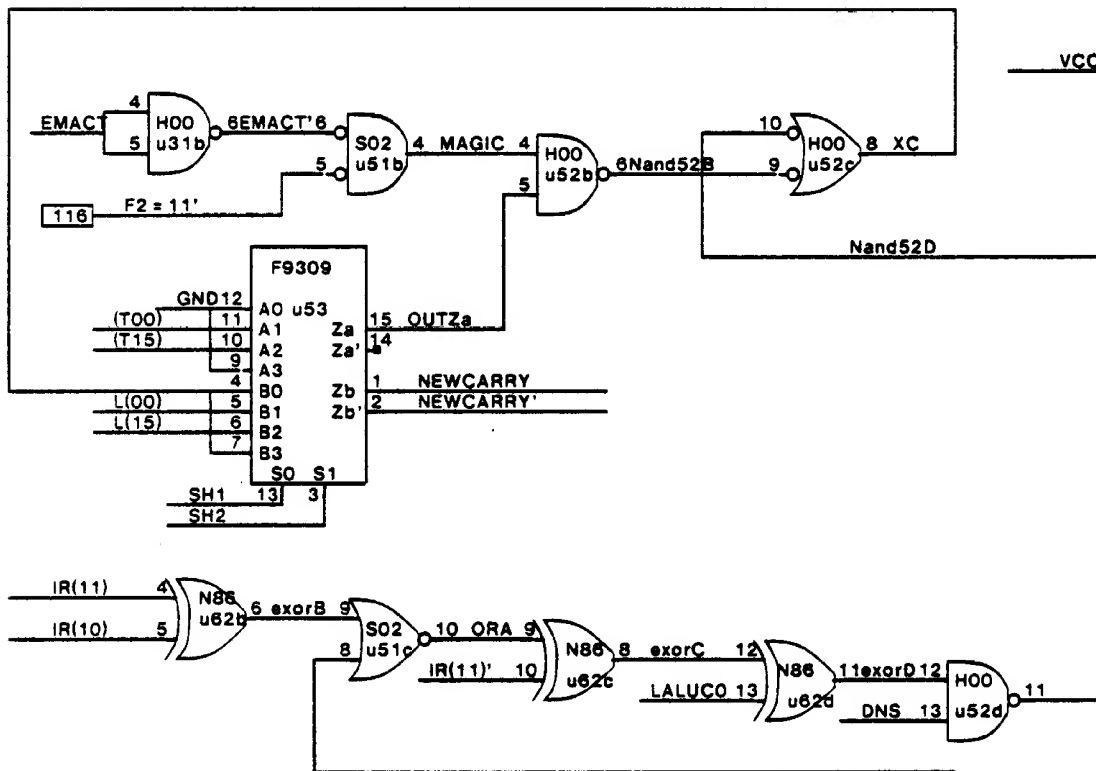
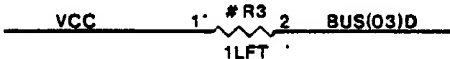
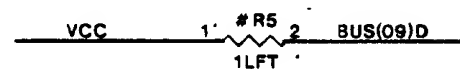
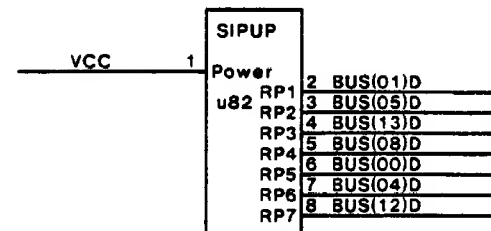
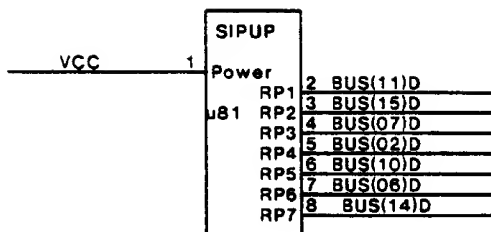
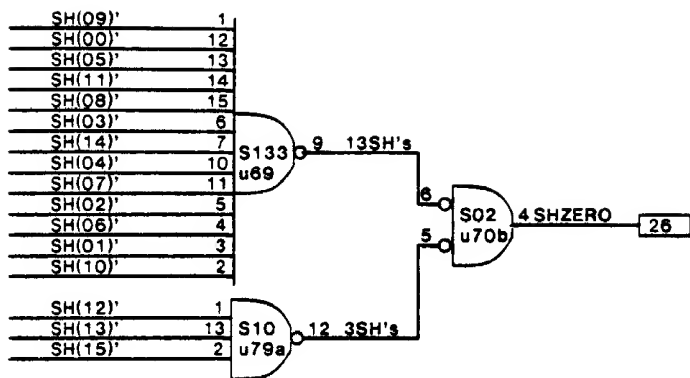












XEROX SPG	Project ALTO II	ASSEMBLY, P.W. ARITHMETIC LOGIC UNIT	File ALU12.sil	Designer LEUNG	Rev A	Date 10/1/80	Page 12
--------------	--------------------	---	-------------------	-------------------	----------	-----------------	------------

